



# THE QUEST FOR LOW LATENCY STORAGE

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# Outline

- The history of storage latency and where we stand today
- The promise of Storage Class Memory (SCM) and 3D Xpoint™ Memory
- Extensive compute platform changes driven by the quest for lower storage latency with SCM / 3D Xpoint™ Memory
  - As traditional storage
  - As persistent memory
- Innovation opportunities abound

# 1956: IBM RAMAC 350

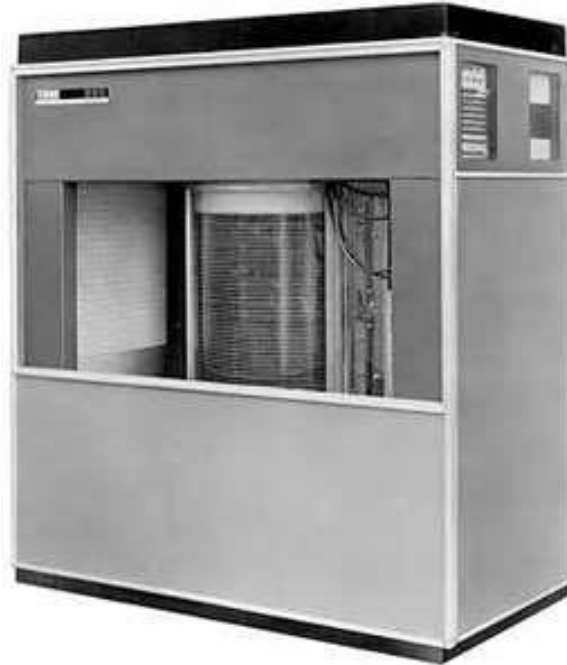
5 MBytes

\$57,000

\$15200/Mbyte

~1.5 Random IOPs\*

600ms latency

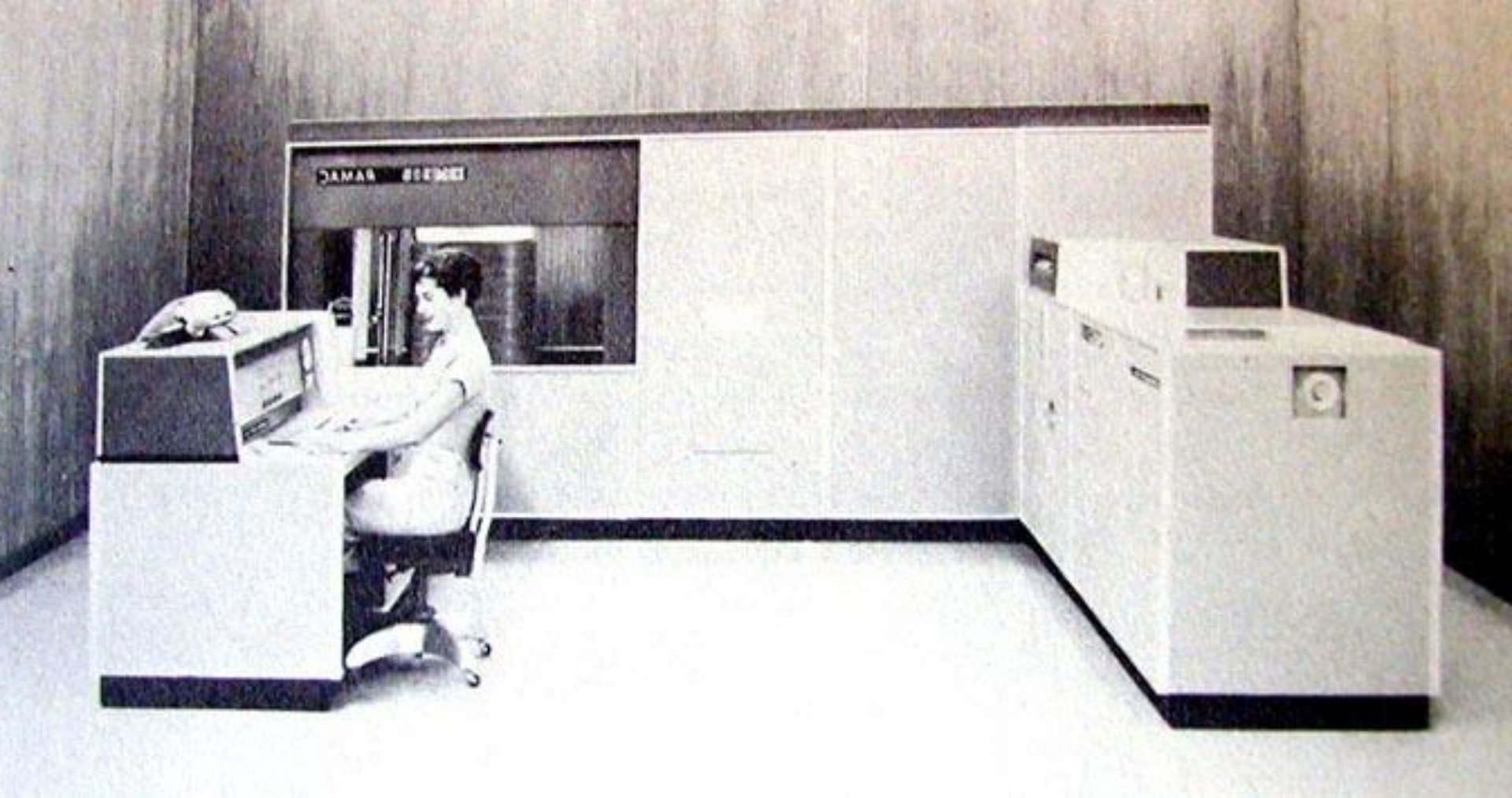


\* IOPs depends on the workload and is a range

\*Other names and brands may be claimed as the property of others.







# 1980: IBM 3350

300 Mbytes

\$60,000

\$200/MByte

30 random IOPs

33ms latency





# 1983: IBM3380

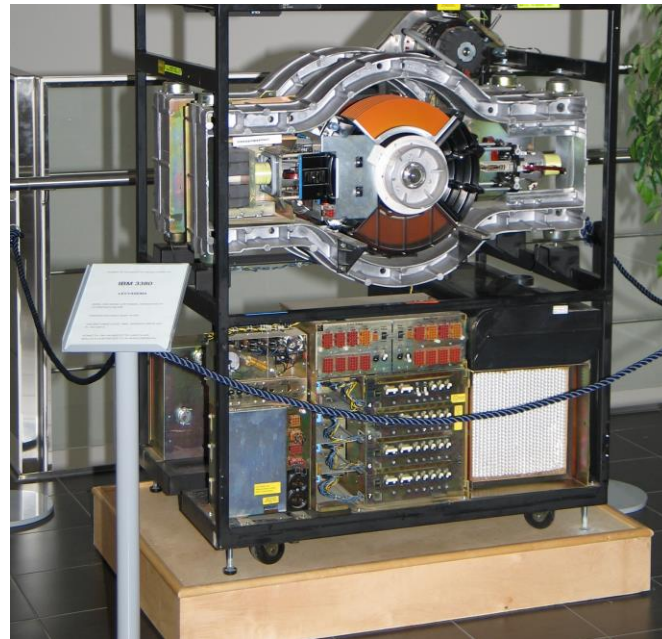
2.52 GBytes

\$82,000

\$36/MByte

~160 IOPS total

25ms latency



Two hard disk assemblies each with two independent actuators  
each accessing 630 MB gigabyte within one chassis

# 2007: 15K RPM HDD

15K RPM HDD

About 200 random IOPs\*

~5ms latency



IOPS scaling problem was addressed through HDDs in parallel in Enterprise

\* IOPs depends on the workload and is a range



# 2016: 10K RPM HDD

1.8TB

~150 IOPs

6.6ms latency



# 2016 NVMe NAND SSD

2TB

500,000+ IOPs

~60 usec latency



# The Continuing Need For Lower Latency

RAMAC 350  
600ms



~100x

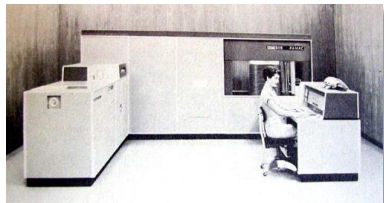
Access time reduction

~10,000x

Access time reduction

59 Years

RAMAC 305  
100 Hz best  
case "clock"



~40,000,000x

Clock speed increase



10K RPM  
~6ms access



NAND SSD  
~60us access



Core™ i7  
~4 Ghz clock

# Lower Storage Latency Requires Media and Platform Improvements



First HDD



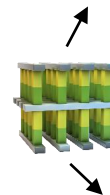
Modern HDD



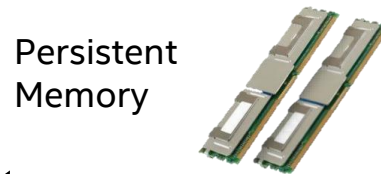
NAND SSD



NVMe NAND SSD



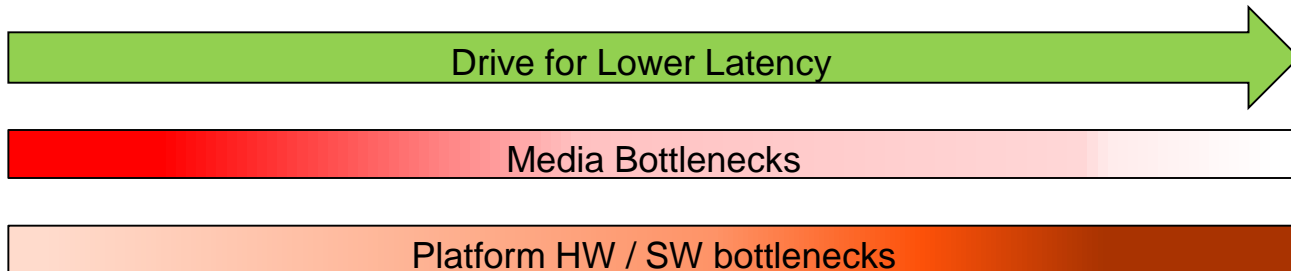
3D XPoint™  
memory (SCM)



Persistent  
Memory

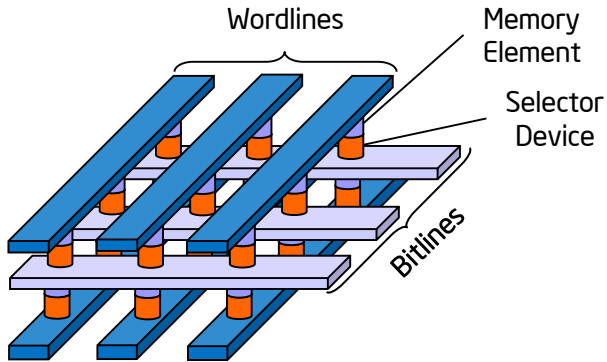


Ultra fast SSD



# Addressing Media Latency: Next Gen NVM / SCM

## Scalable Resistive Memory Element



Cross Point Array in Backend Layers  $\sim 4\lambda^2$  Cell

## Resistive RAM NVM Options

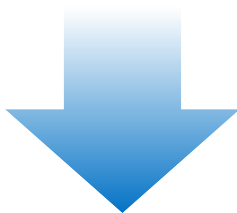
Family	Defining Switching Characteristics
Phase Change Memory	Energy (heat) converts material between crystalline (conductive) and amorphous (resistive) <u>phases</u>
Magnetic Tunnel Junction (MTJ)	Switching of magnetic resistive layer by <u>spin-polarized electrons</u>
Electrochemical Cells (ECM)	Formation / dissolution of "nano-bridge" by <u>electrochemistry</u>
Binary Oxide Filament Cells	Reversible filament formation by <u>Oxidation-Reduction</u>
Interfacial Switching	<u>Oxygen vacancy drift</u> diffusion induced barrier modulation

**Scalable, with potential for near DRAM access times**

# 3D XPoint™ Technology

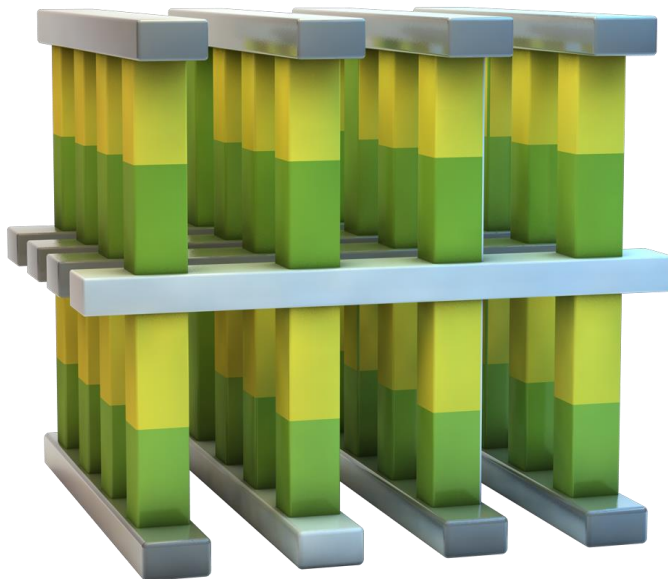
## Crosspoint Structure

Selectors allow dense packing and individual access to bits



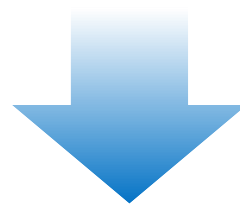
## Scalable

Memory layers can be stacked in a 3D manner



## Breakthrough Material Advances

Compatible switch and memory cell materials



## High Performance

Cell and array architecture that can switch states 1000x faster than NAND



# A NEW CLASS OF NON-VOLATILE MEMORY



**1000X**  
**FASTER**  
THAN NAND



**1000X**  
**ENDURANCE**  
OF NAND

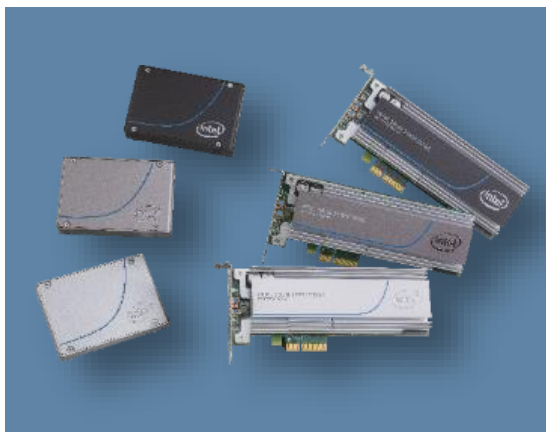


**10X**  
**DENSER**  
THAN DRAM

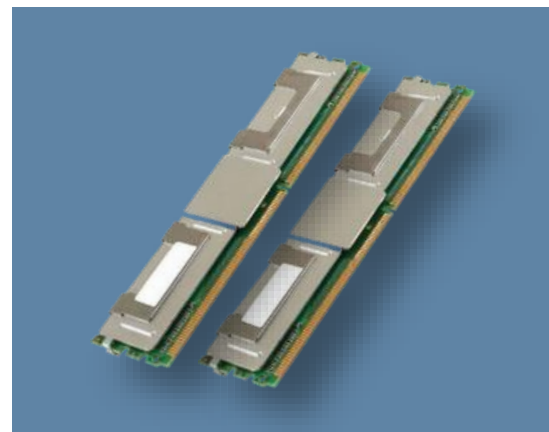
\*Results have been estimated or simulated using internal analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance

# 3D XPoint™ Technology Instantiation

## INTEL® OPTANE™ SSDS



## DIMMS BASED ON 3D XPOINT™



# 3D Xpoint™ Technology Video

Please excuse the marketing

# 3D Xpoint™ Technology Video



# Demonstration of 3D Xpoint™ SSD Prototype

## NAND TECHNOLOGY

Intel® SSD DC P3700 Series



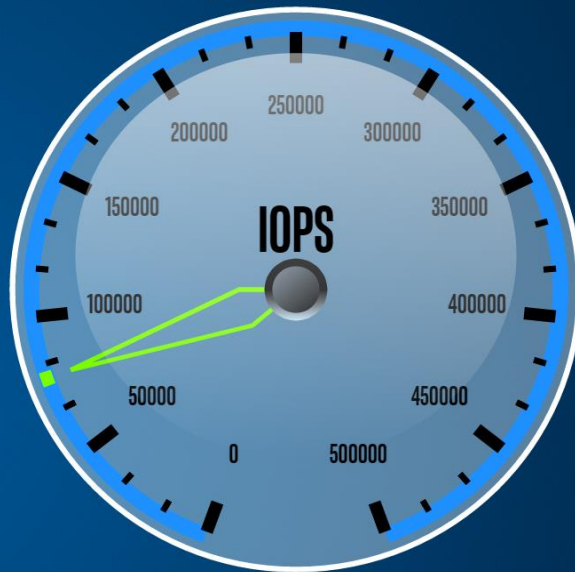
IOPS  
**10,700**

**7.32X**  
IOPS  
PERFORMANCE

READ  
QUEUE DEPTH  
**1**

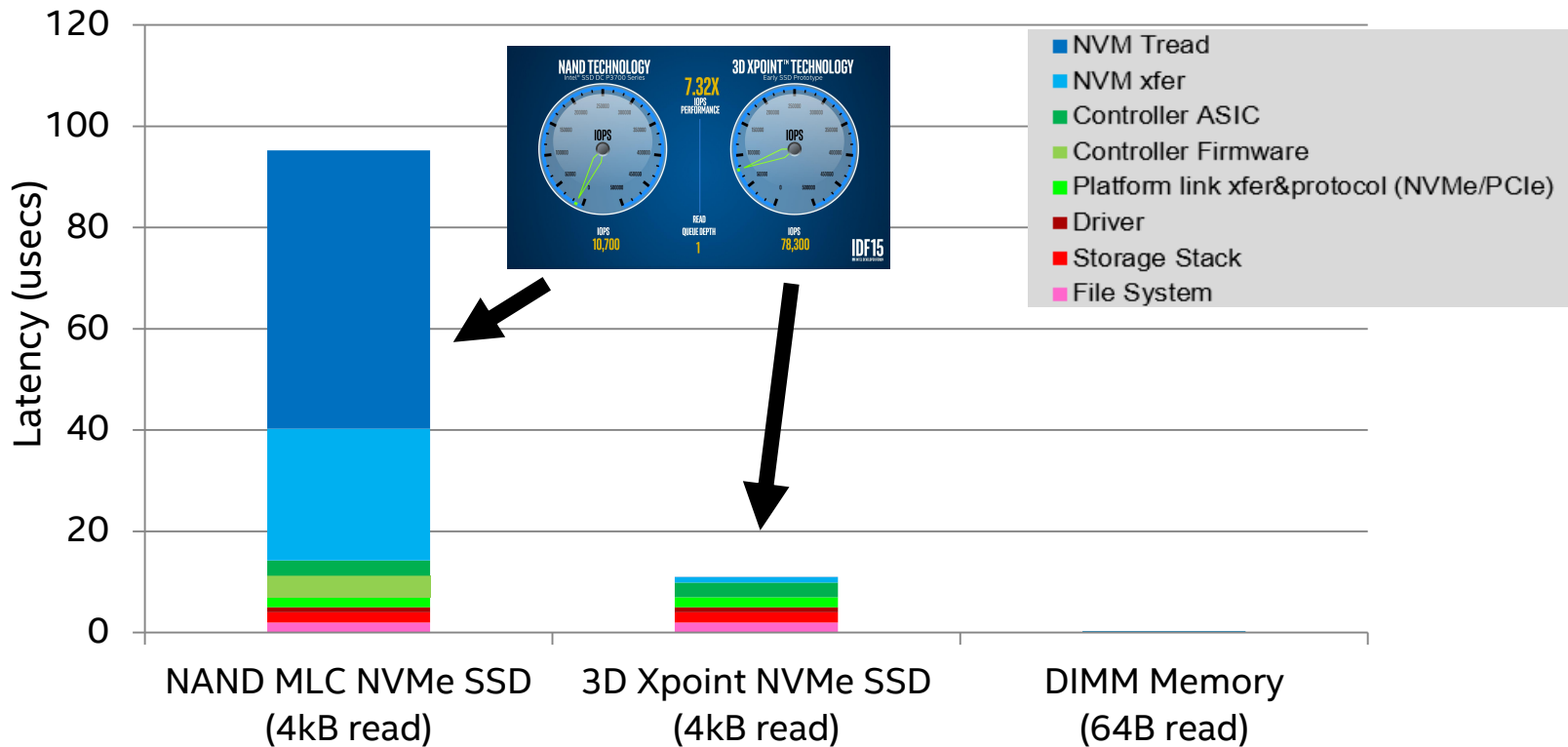
## 3D XPOINT™ TECHNOLOGY

Early SSD Prototype



IOPS  
**78,300**

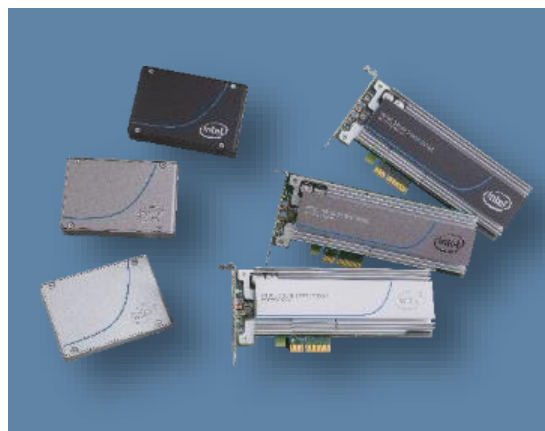
# Need to Address System Architecture To Go Lower



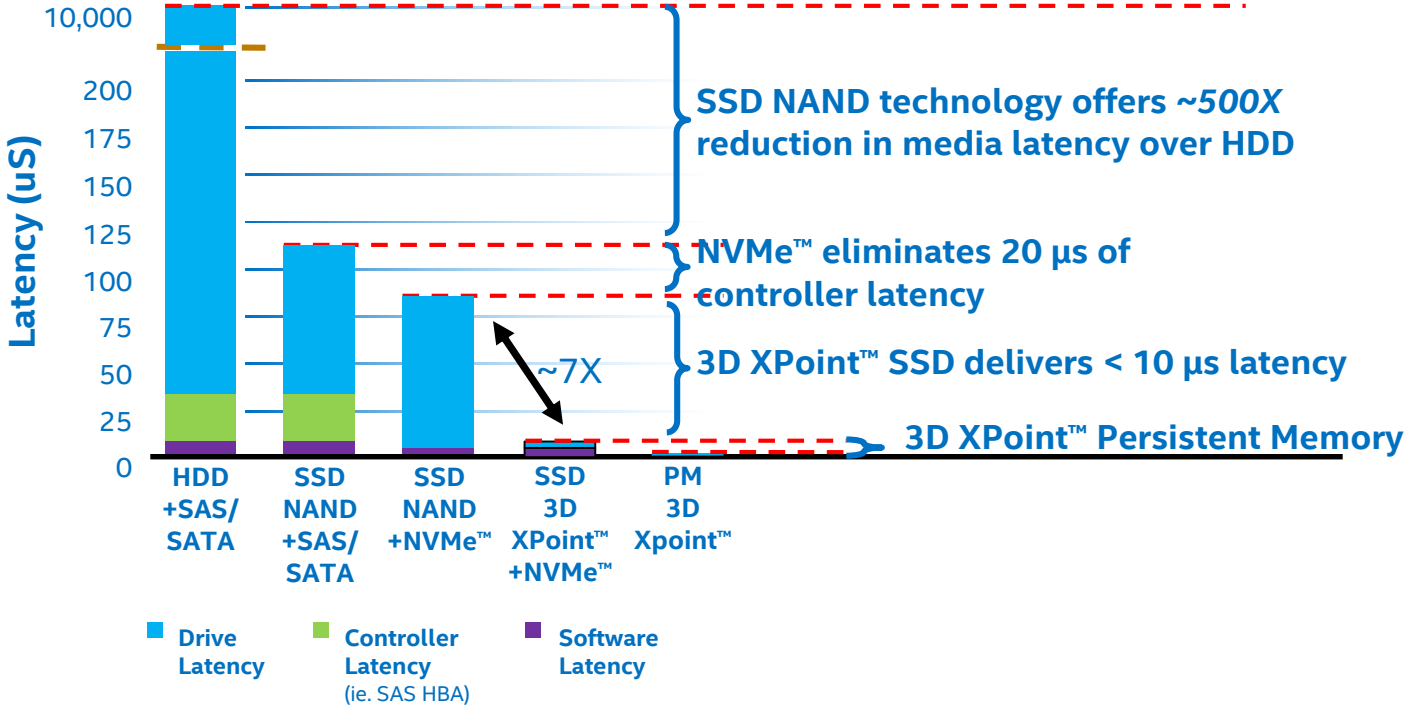


# Block Storage Platform Changes

## INTEL® OPTANE™ SSDS

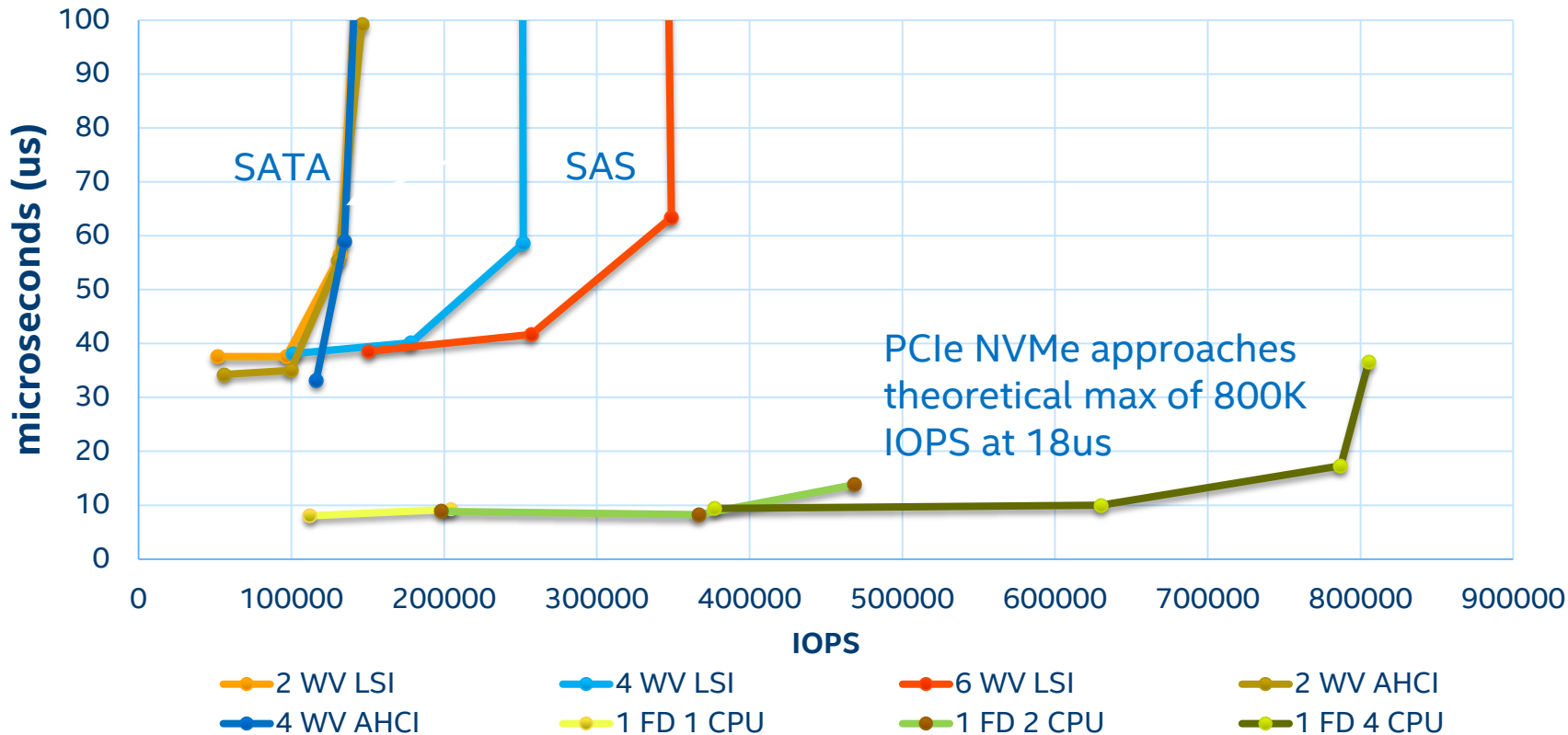


# Addressing Interface Efficiency With NVMe / PCI

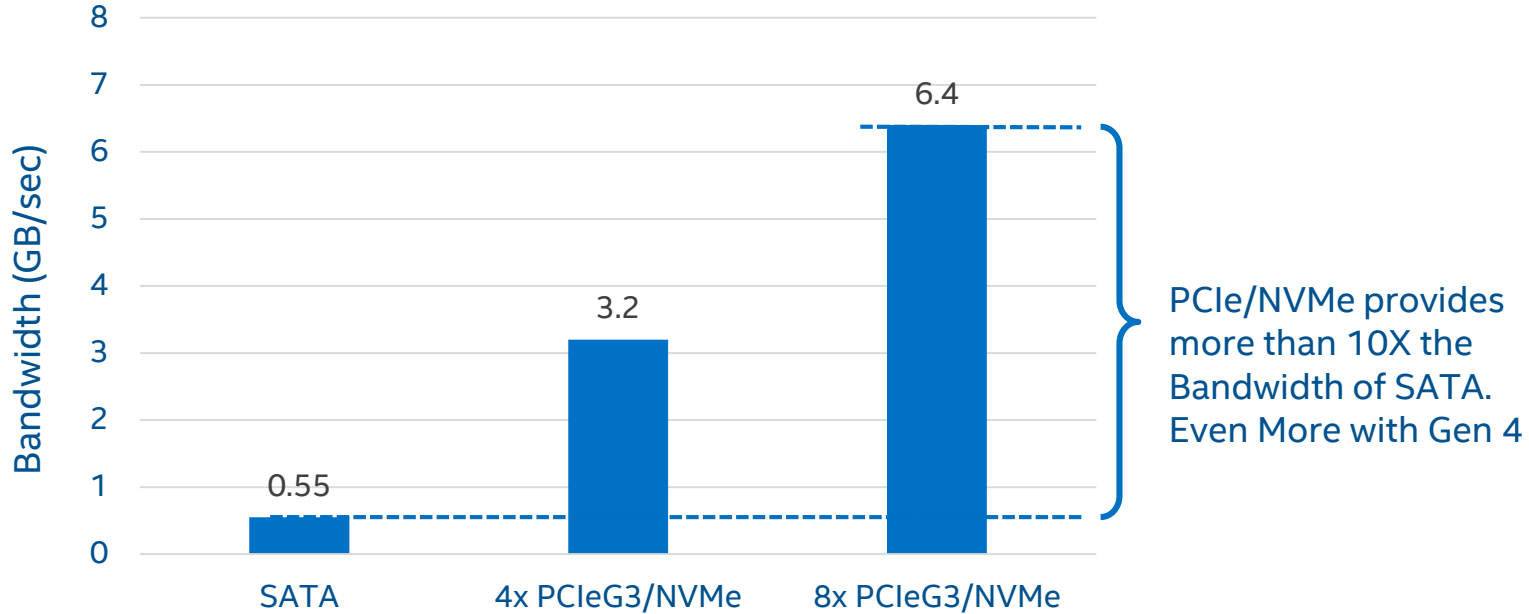


# NVMe Delivers Superior Latency

Platform HW/SW Average Latency Excluding Media 4KB



# NVMe/PCIe Provides More Bandwidth

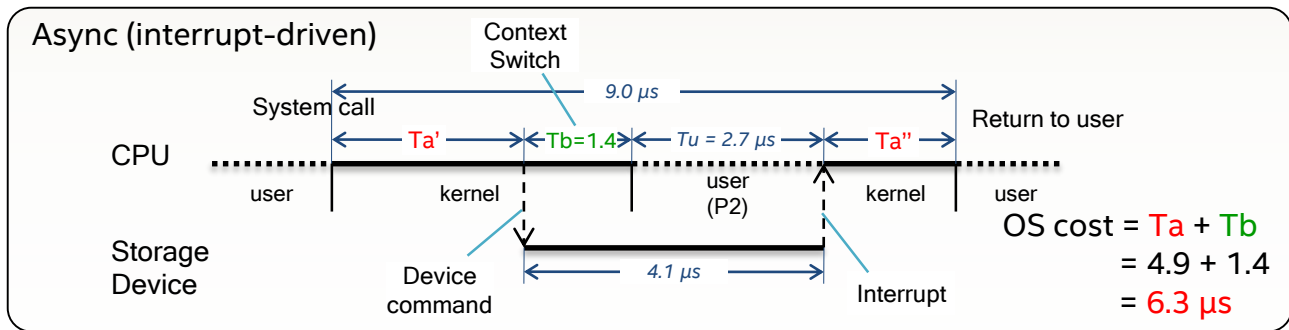


# Storage SW Stack Optimizations

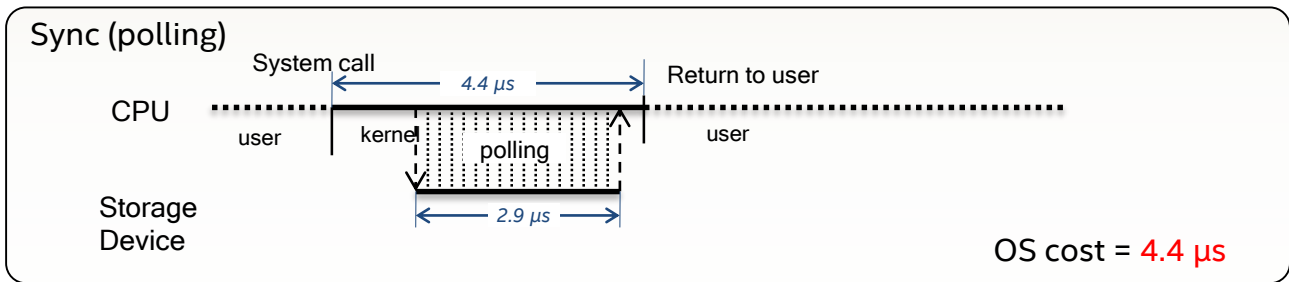
Much of the storage stack designed with HDDs latencies in mind

- No point in optimizing until now
- Example: Paging algorithms with seek optimization and grouping

# Synchronous Completion for Queue Depth 1?



From Yang: FAST '12  
-10th USENIX  
Conference on File  
and Storage  
Technologies



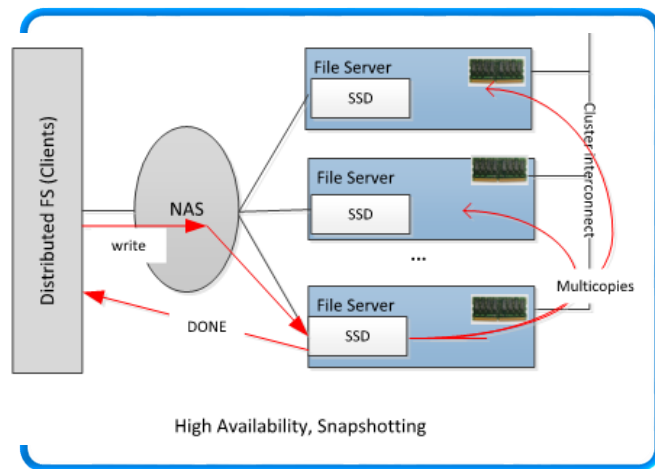


# Standards for Low Latency Replication

In most Datacenter usage models, a storage write does not “count” until replicated

High replication overhead diminishes the performance differentiation of 3D XPoint™ technology

NVMe over Fabrics is a developing SNIA specification for low overhead replication



# Summary: Block Storage Platform Changes

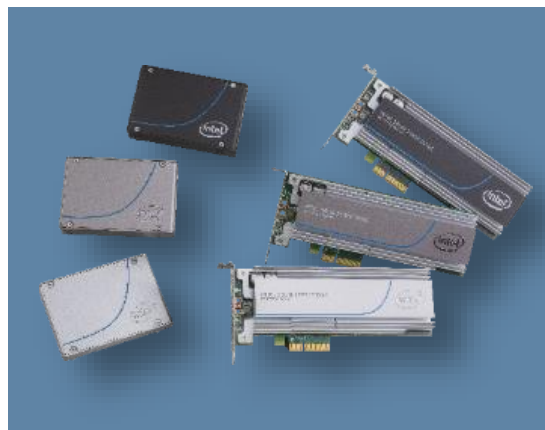
Move to PCIe based storage

Streamlined command set NVMeexpress

OS / SW stack optimizations

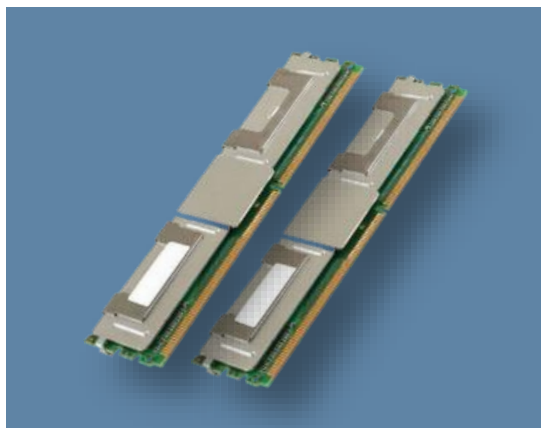
Fast replication standards

**INTEL® OPTANE™ SSDS**



# Persistent Memory Oriented Platform Changes

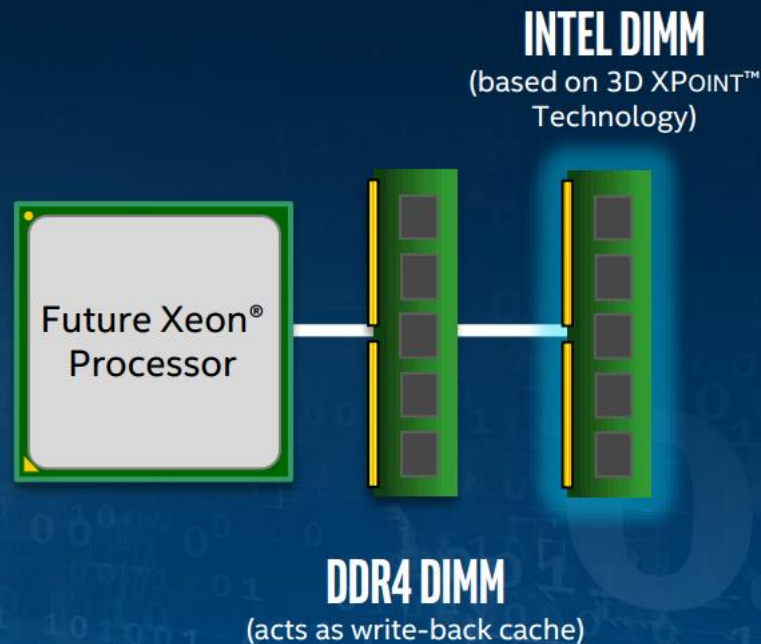
## **DIMMS BASED ON 3D XPOINT™**



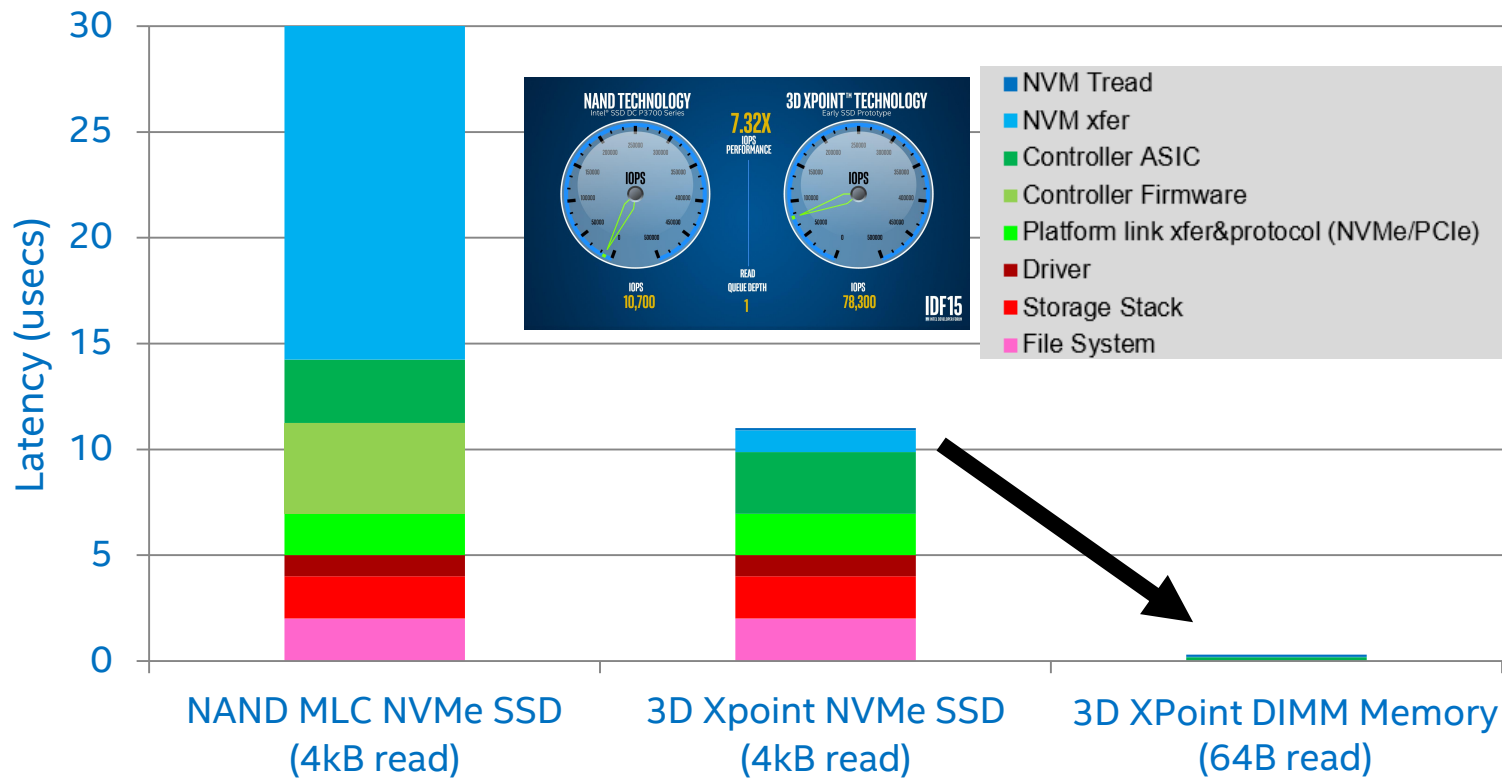
# INTEL DIMMs

*Based on 3D XPoint™ Technology*

- DDR4 electrical & physical compatible
- Required support delivered by next generation Intel® Xeon® platform
- Up to 4X system memory capacity, at significantly lower cost than DRAM
- Can deliver big memory benefits without modifications to OS or applications



# Why Persistent Memory?



# Open NVM Programming Model



SNIA Technical Working Group  
Initially defined 4 programming modes required by developers

Spec 1.0 developed, approved by SNIA voting members and published

Interfaces for PM-aware file system accessing kernel PM support

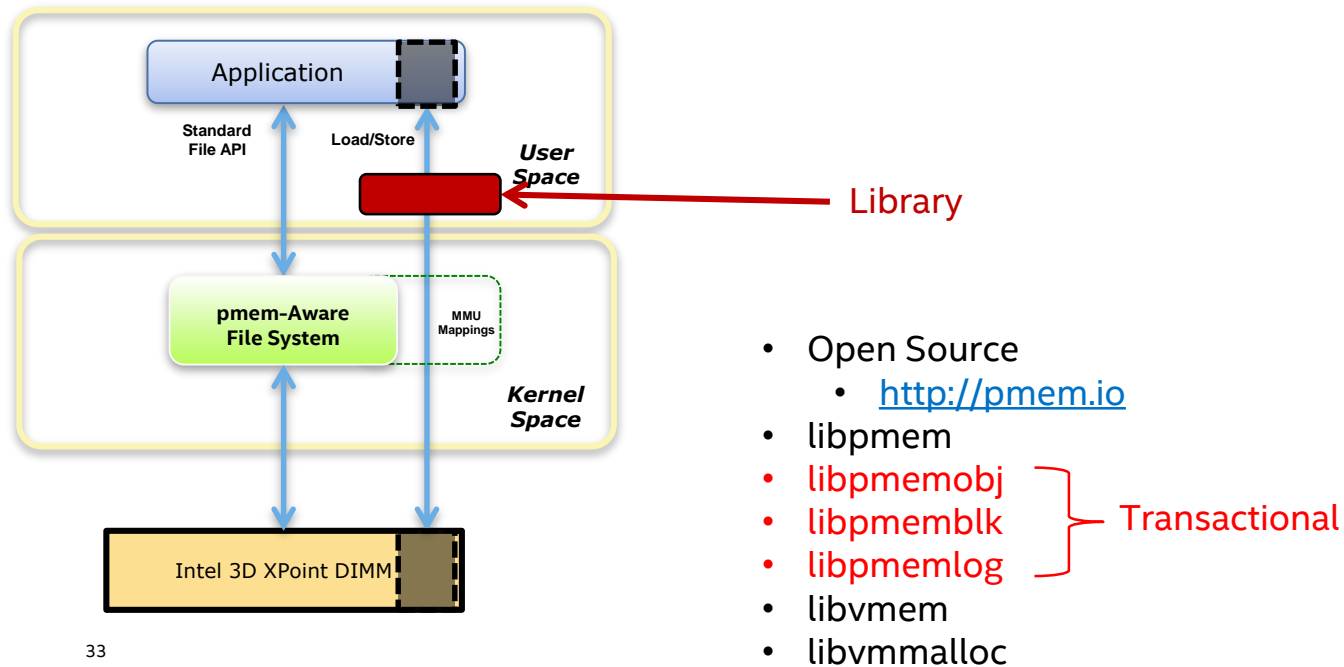
interfaces for application accessing a PM-aware file system

Kernel support for block NVM extensions

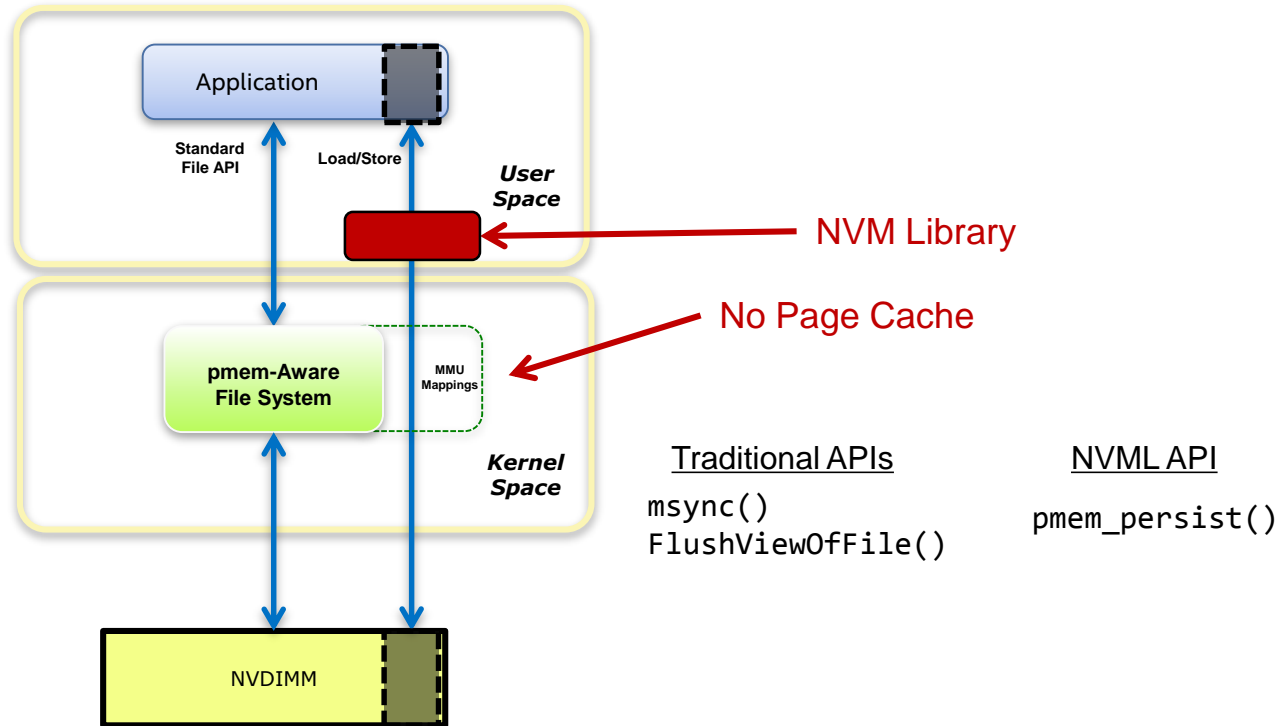
Interfaces for legacy applications to access block NVM extensions

# NVM Library: pmem.io

64-bit Linux Initially



# Write I/O Replaced with Persist Points





# Operating System Support for Persistent Memory

**SDC** 15

STORAGE DEVELOPER CONFERENCE

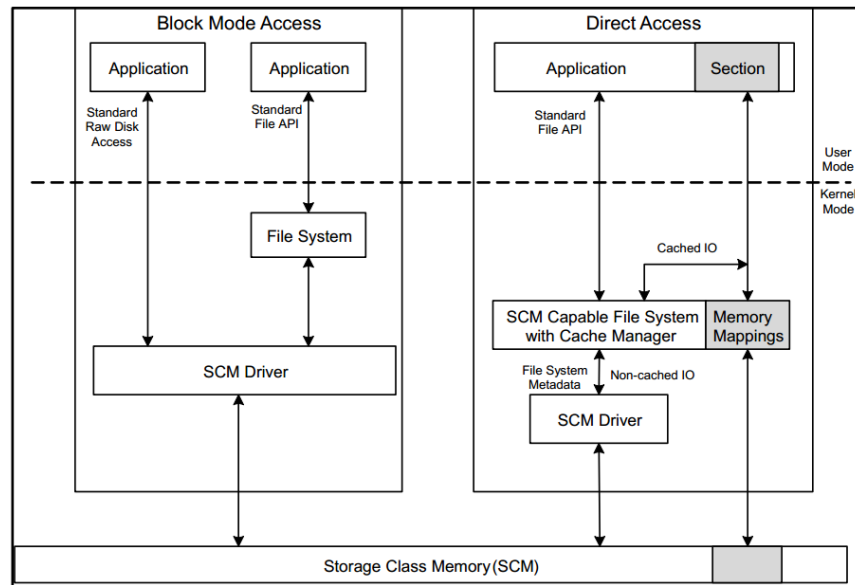
SNIA ■ SANTA CLARA, 2015

## Storage Class Memory Support in the Windows Operating System

Neal Christiansen

Principal Development Lead  
Microsoft

nealch@microsoft.com

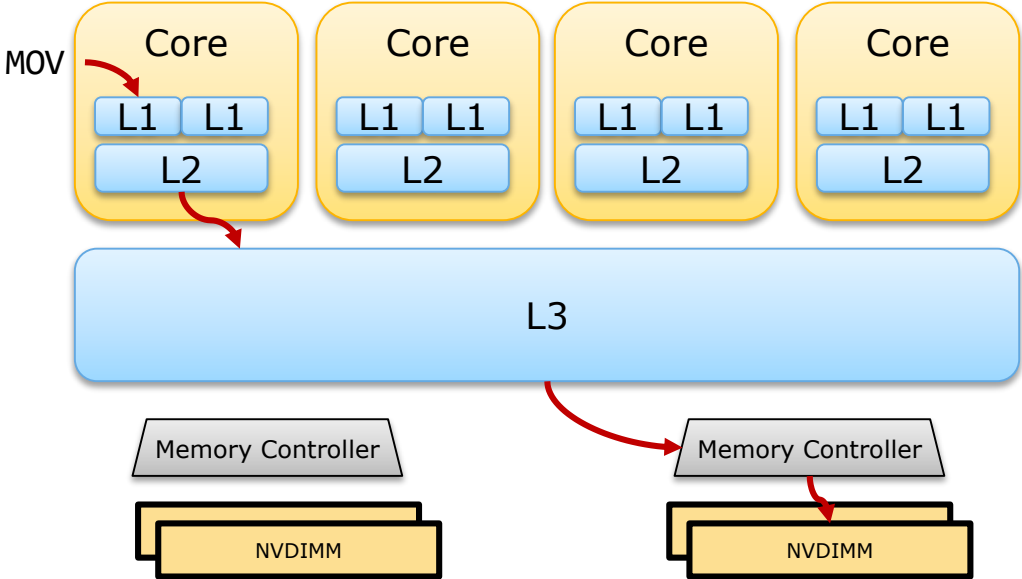


**SDC** 15

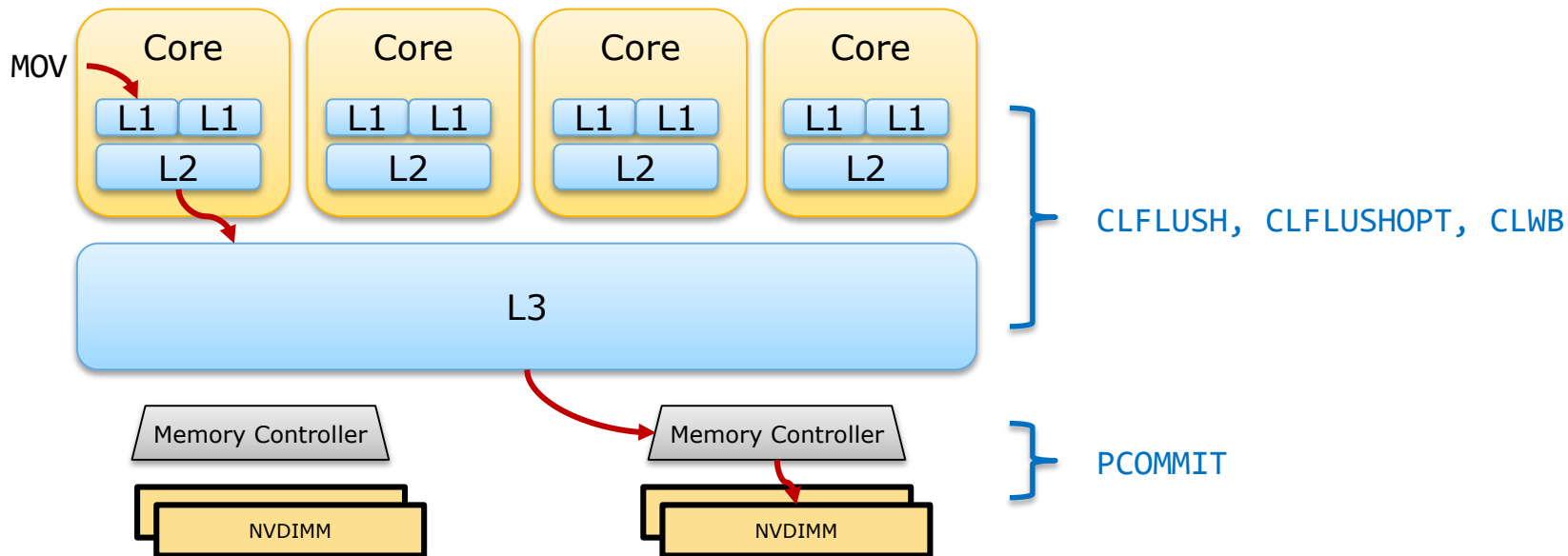
2015 Storage Developer Conference. © Microsoft. All Rights Reserved.



# The Data Path



# New Instructions For Flushing Writes



# Flushing Writes from Caches

Instruction	Meaning
CLFLUSH addr	Cache Line Flush: Available for a long time
CLFLUSHOPT addr	Optimized Cache Line Flush: New to allow concurrency
CLWB addr	Cache Line Write Back: Leave value in cache for performance of next access

# Flushing Writes from Memory Controller

Instruction	Meaning
PCOMMIT	Persistent Commit: Flush stores accepted by memory subsystem
Asynchronous DRAM Refresh	Flush outstanding writes on power failure <b>Platform-Specific Feature</b>

# Example Code

	<u>Comments</u>
<code>MOV X1, 10</code>	} X2,X1 are in pmem
<code>MOV X2, 20</code>	
<code>.</code>	
<code>MOV R1, X1</code>	} Stores to X1 and X2 are globally visible, but <b>may not</b> be persistent
<code>.</code>	
<code>.</code>	
<code>CLFLUSHOPT X1</code>	} X1 and X2 moved from caches to memory
<code>CLFLUSHOPT X2</code>	
<code>.</code>	
<code>SFENCE</code>	} Ensures <b>PCOMMIT</b> has completed
<code>PCOMMIT</code>	
<code>.</code>	
<code>SFENCE</code>	

# Join the Discussion about Persistent Memory

Learn about the Persistent Memory programming model

- <http://www.snia.org/forums/ssi/nvmp>

Join the pmem NVM Libraries Open Source project

- <http://pmem.io>

[Read the documents and code supporting ACPI 6.0 and Linux NFIT drivers](#)

- [http://www.uefi.org/sites/default/files/resources/ACPI\\_6.0.pdf](http://www.uefi.org/sites/default/files/resources/ACPI_6.0.pdf)
- <https://git.kernel.org/cgit/linux/kernel/git/djwb/nvdim/git/log/?h=nd>
- <https://github.com/pmem/ndctl>
- <http://pmem.io/documents/>
- <https://github.com/O1org/prd>

[Intel Architecture Instruction Set Extensions Programming Reference](#)

- <https://software.intel.com/en-us/intel-isa-extensions>

Intel 3D XPoint™ Memory

- <http://www.intel.com/content/www/us/en/architecture-and-technology/non-volatile-memory.html>

# Persistent Memory Summary

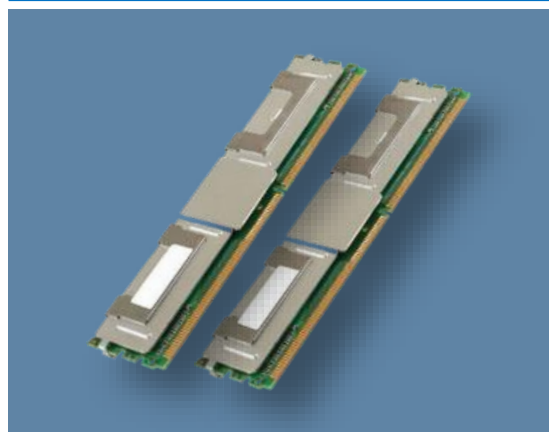
New storage model for low latency

New instructions to support persistence

OS support

Lots of innovation opportunity

**DIMMS BASED ON 3D XPOINT™**





# Low Latency Ahead

